

FIG. 1

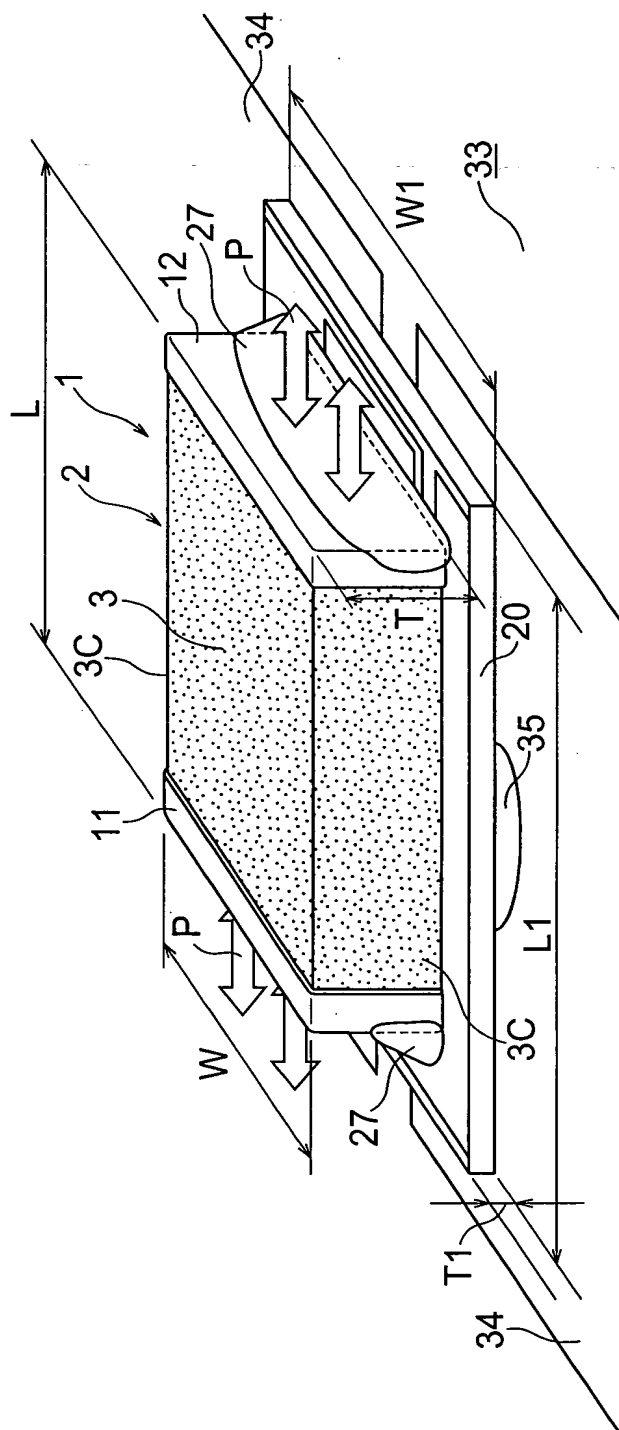


FIG. 2

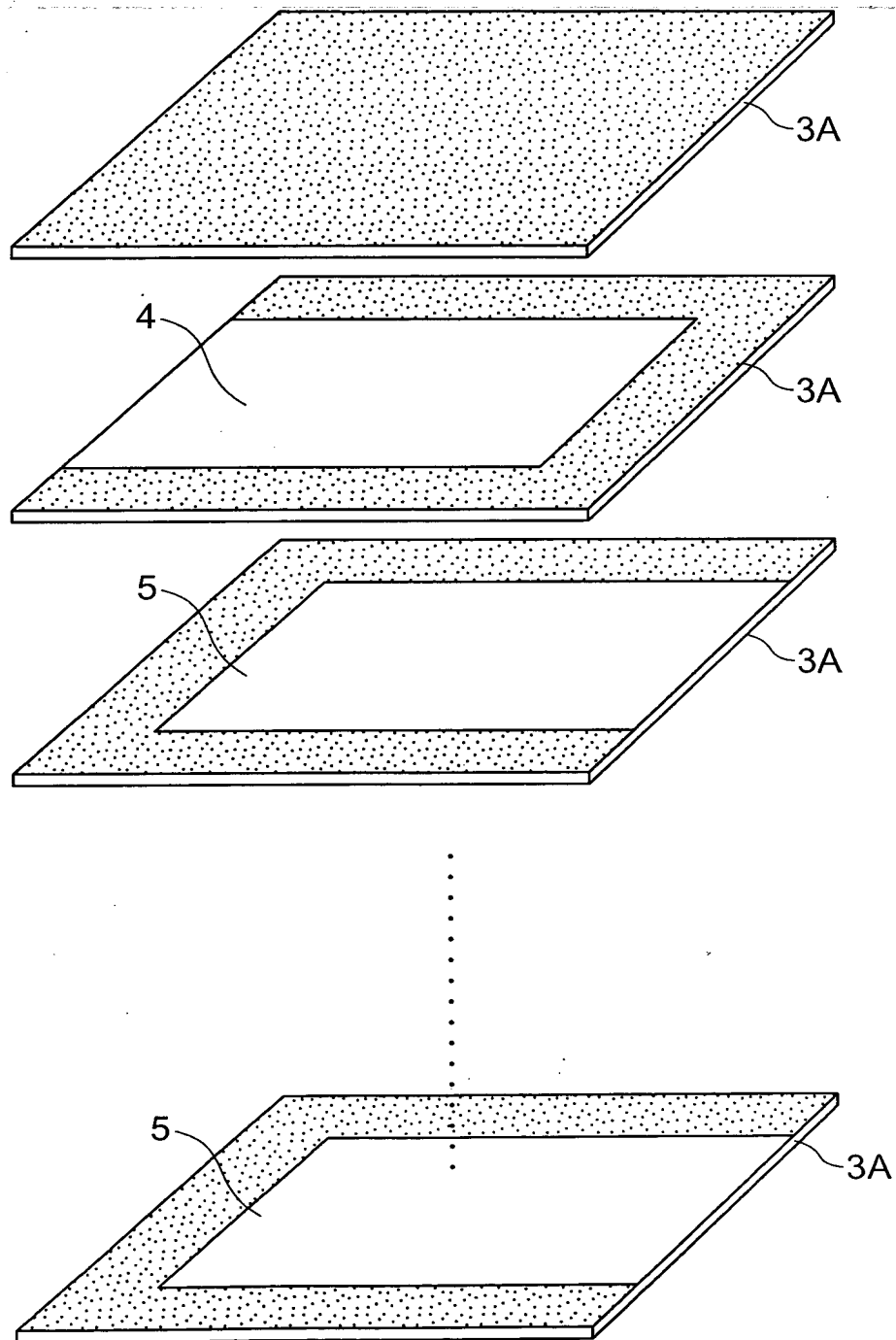


FIG. 3

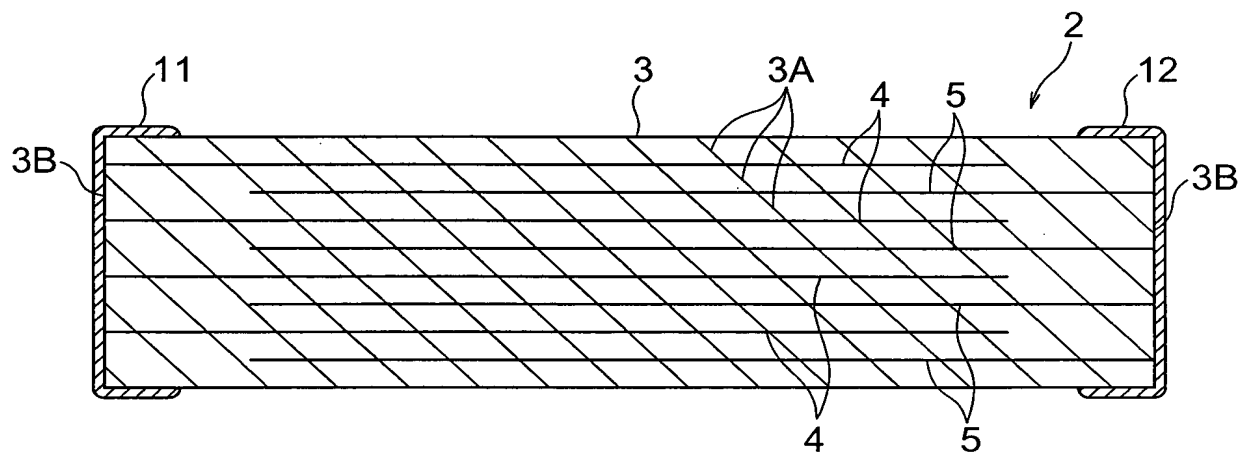


FIG. 4A

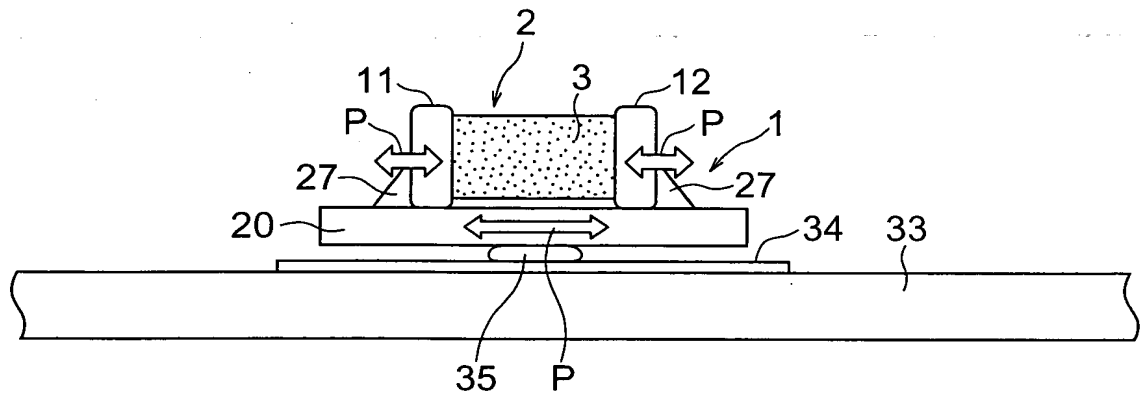


FIG. 4B

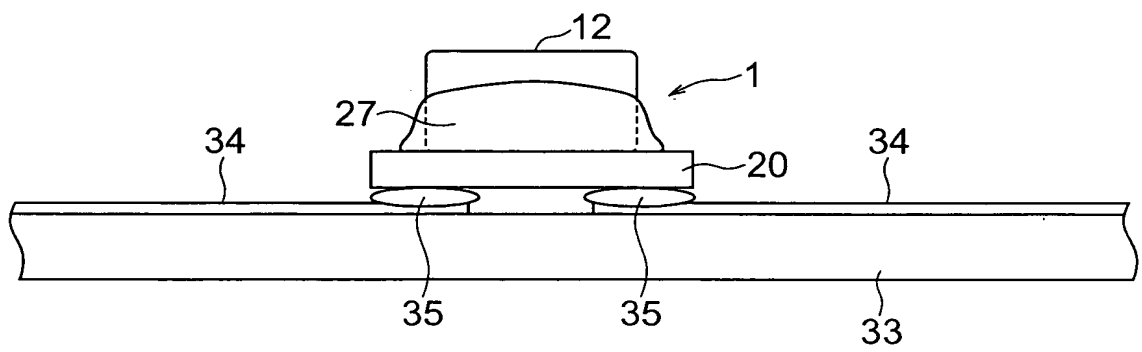


FIG. 5

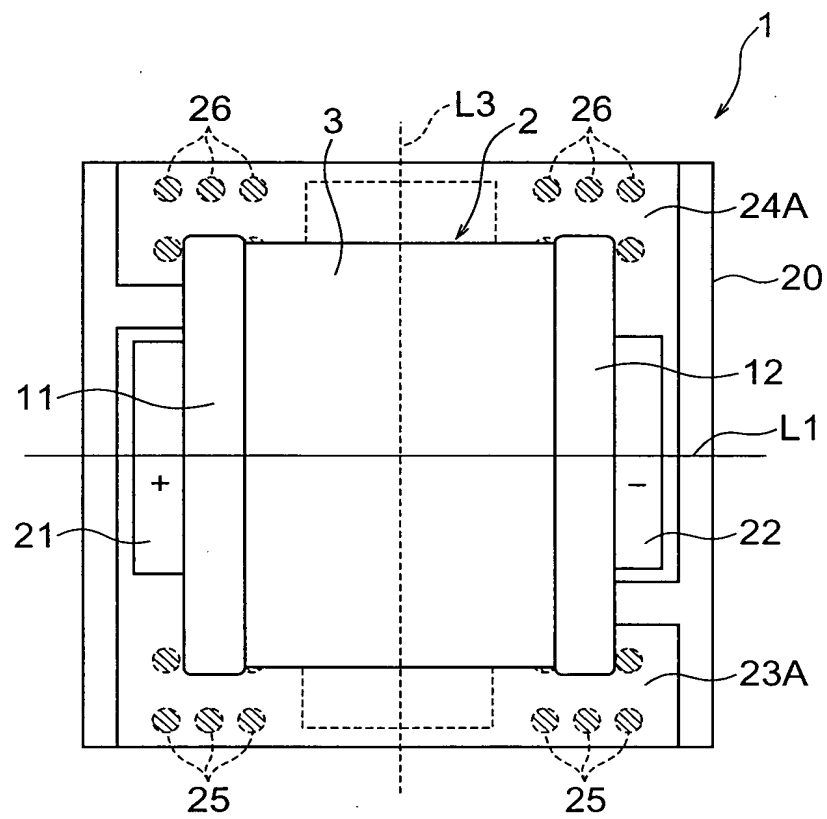


FIG. 6

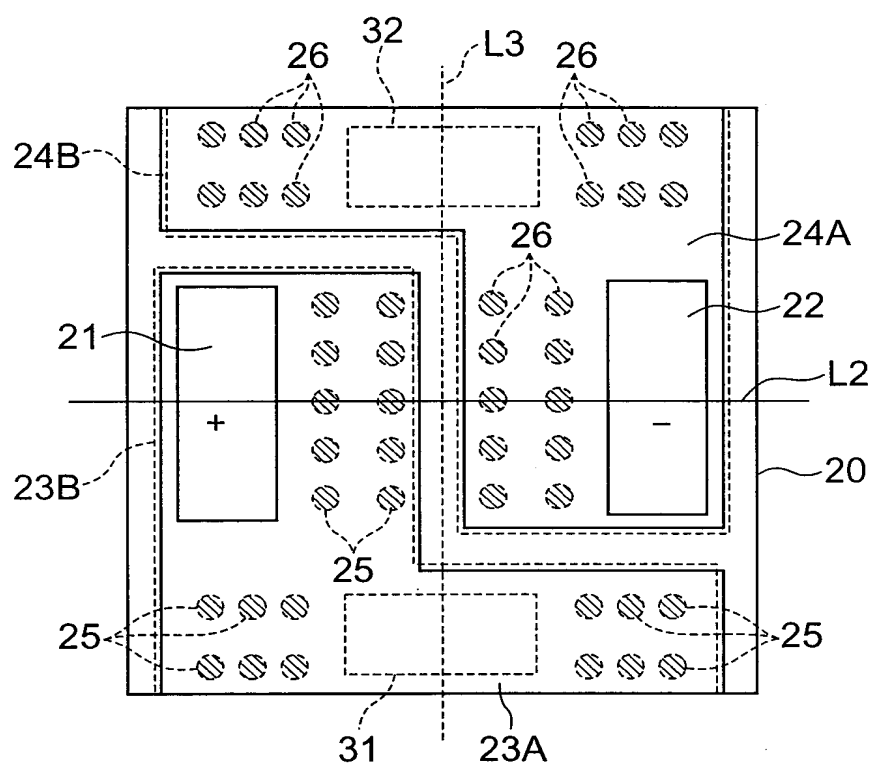


FIG. 7A

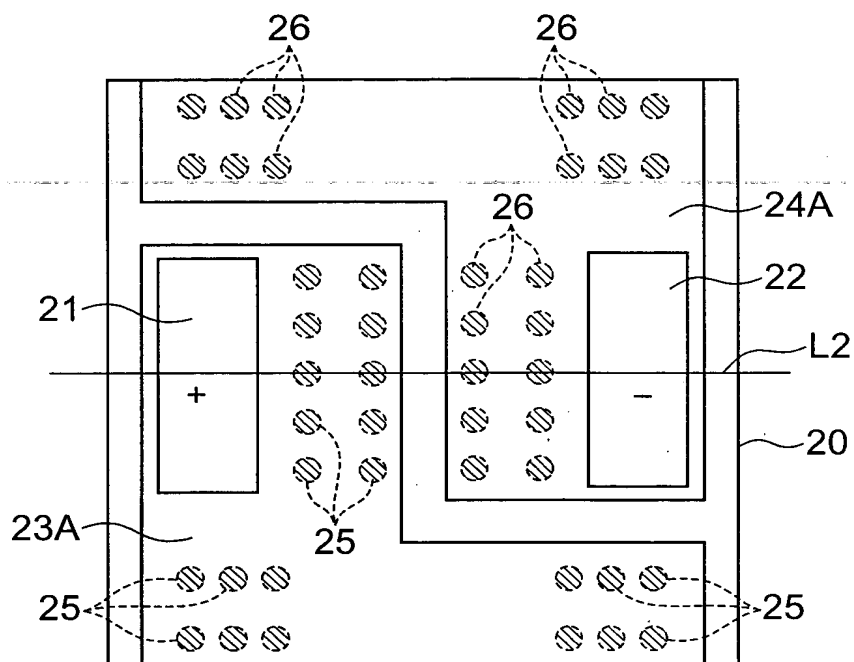


FIG. 7B

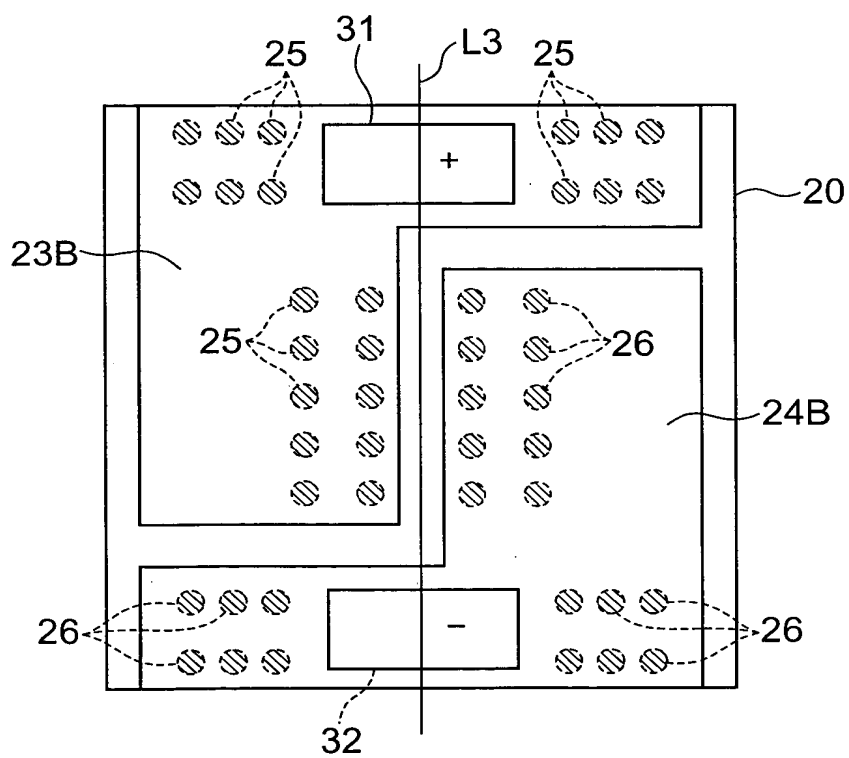


FIG. 8A

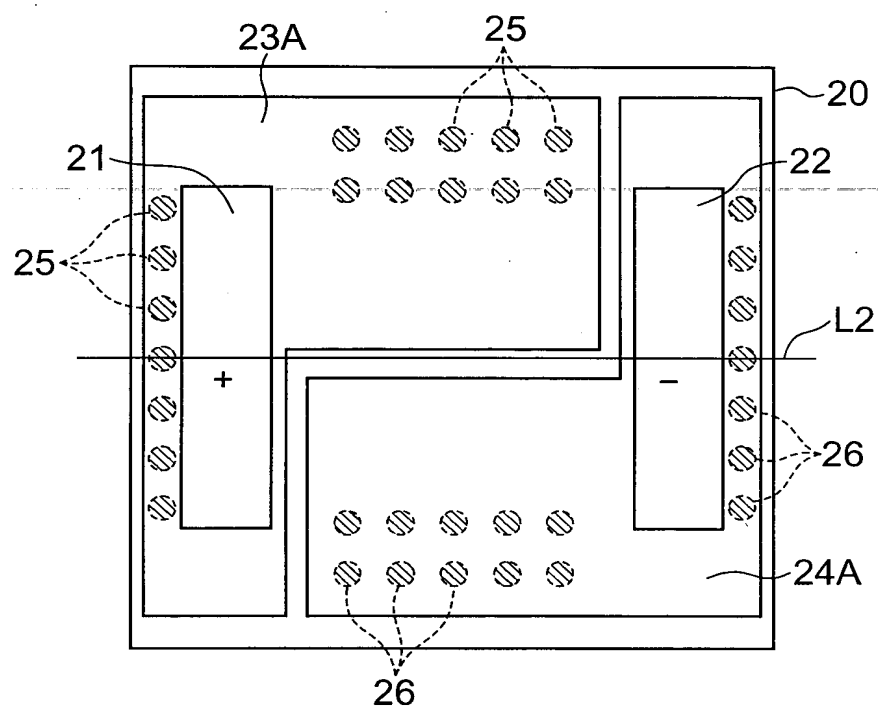


FIG. 8B

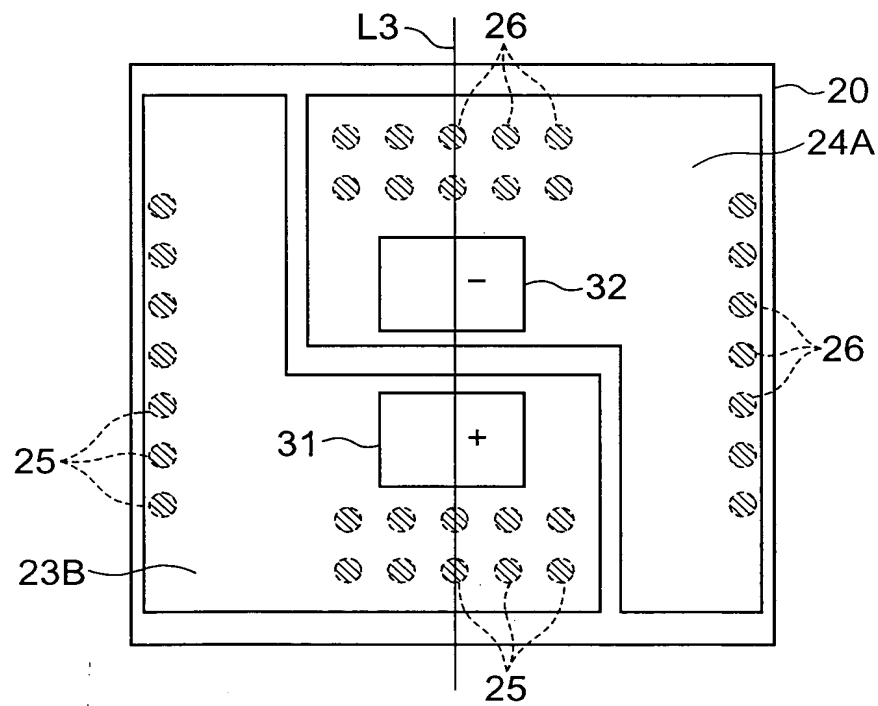


FIG. 9

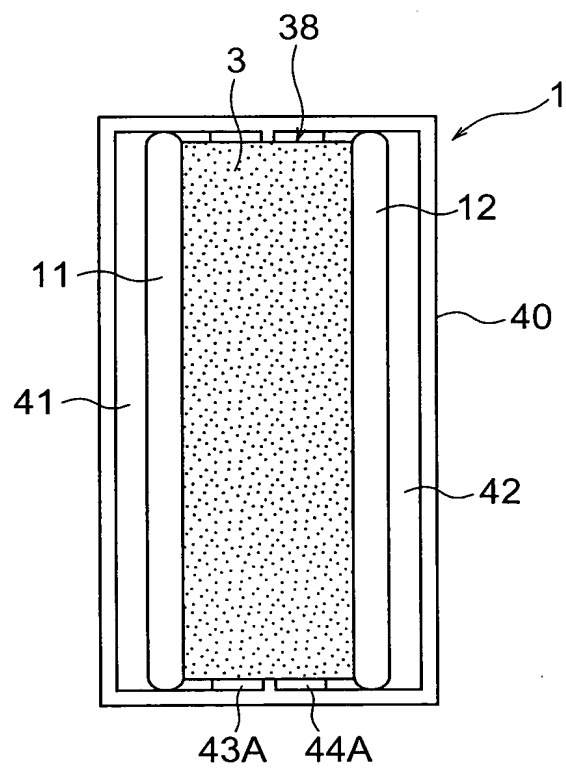


FIG. 10A

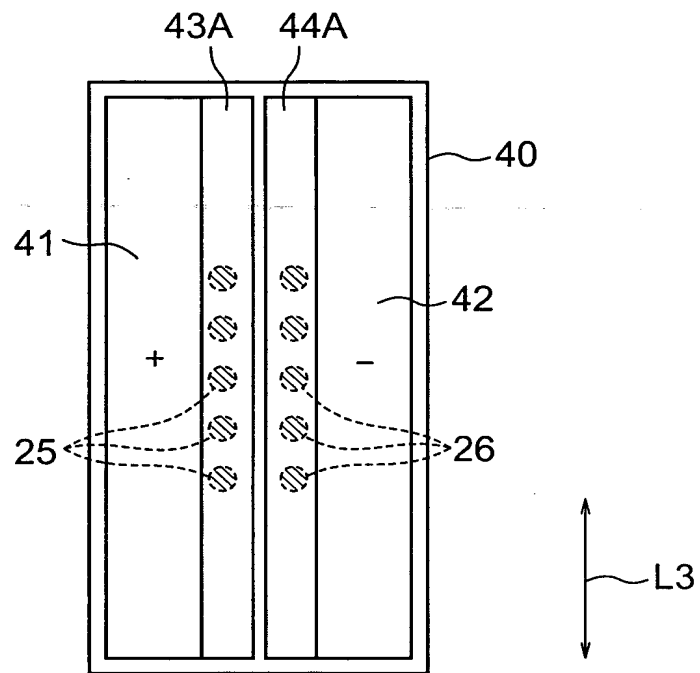


FIG. 10B

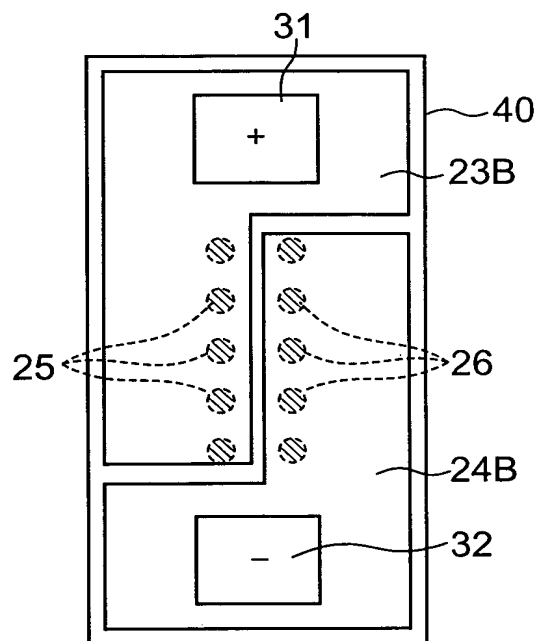


FIG. 11

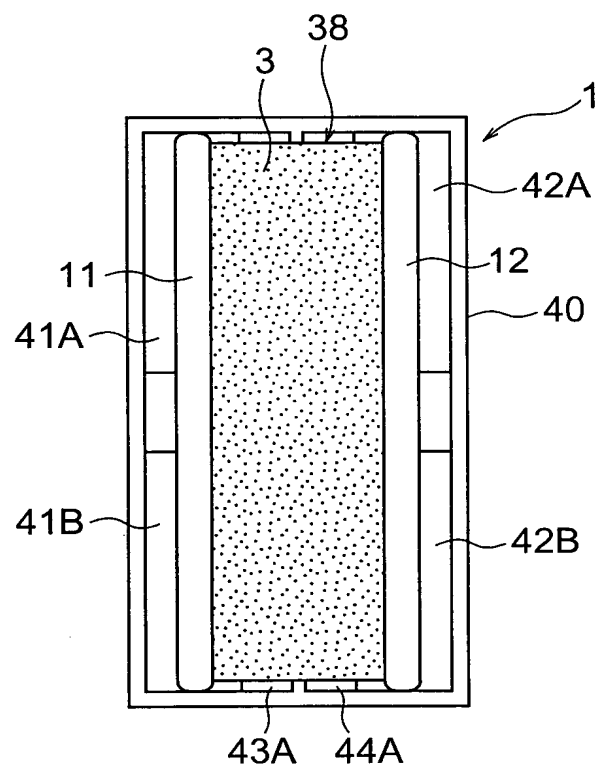


FIG. 12A

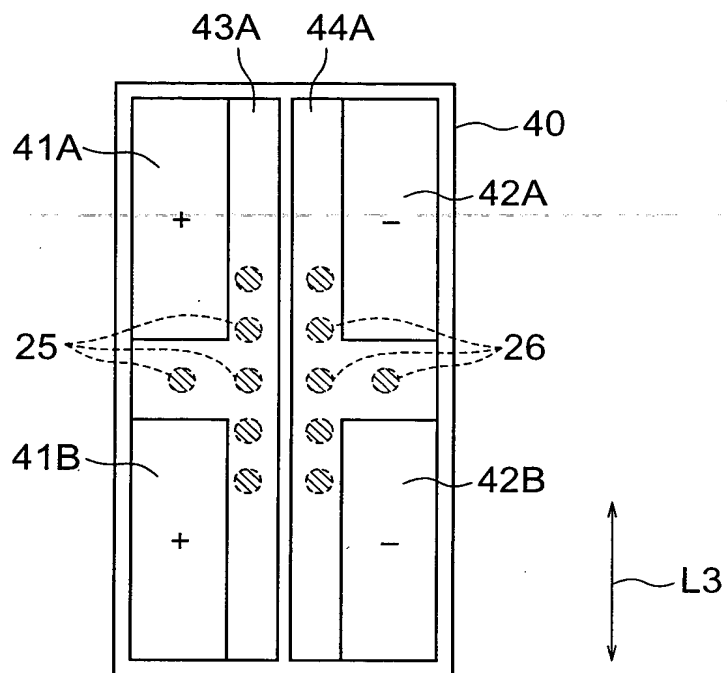


FIG. 12B

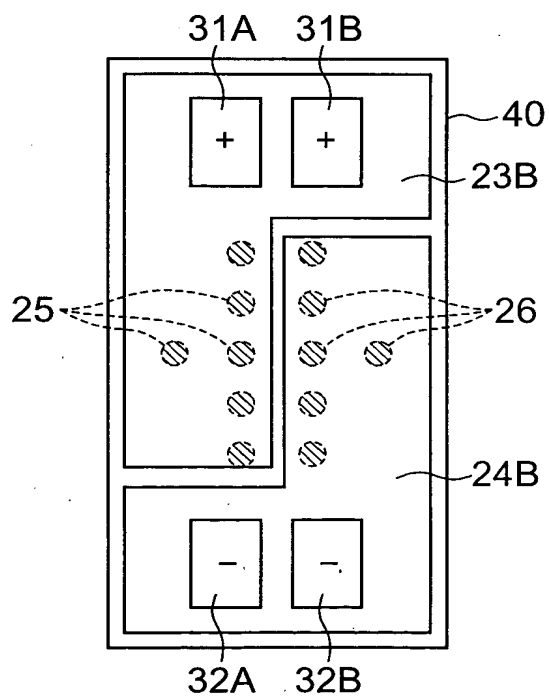


Figure 1 is a plan view of a semiconductor device 20. The device includes a central region 22, a left region 21, a right region 24A, and a bottom region 23A. A central vertical line L2 passes through the center. Various electrodes are shown, including 25, 26, 46, 47, and 48. The central region 22 contains a negative sign (-), while the left region 21 contains a positive sign (+). The bottom region 23A also contains a positive sign (+). The electrodes are arranged in a grid-like pattern, with some electrodes (25, 26) having dashed lines indicating connections or paths.

FIG. 14A

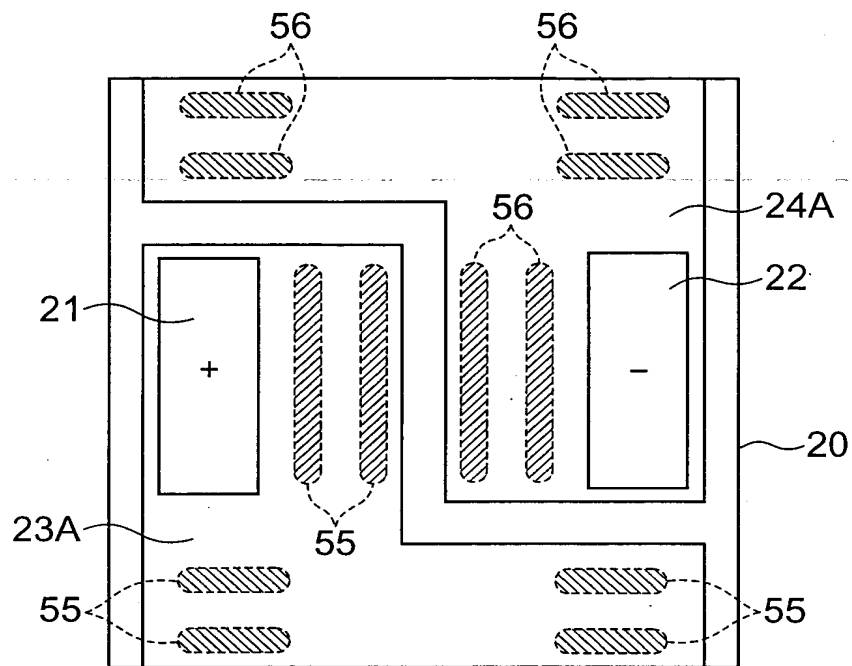


FIG. 14B

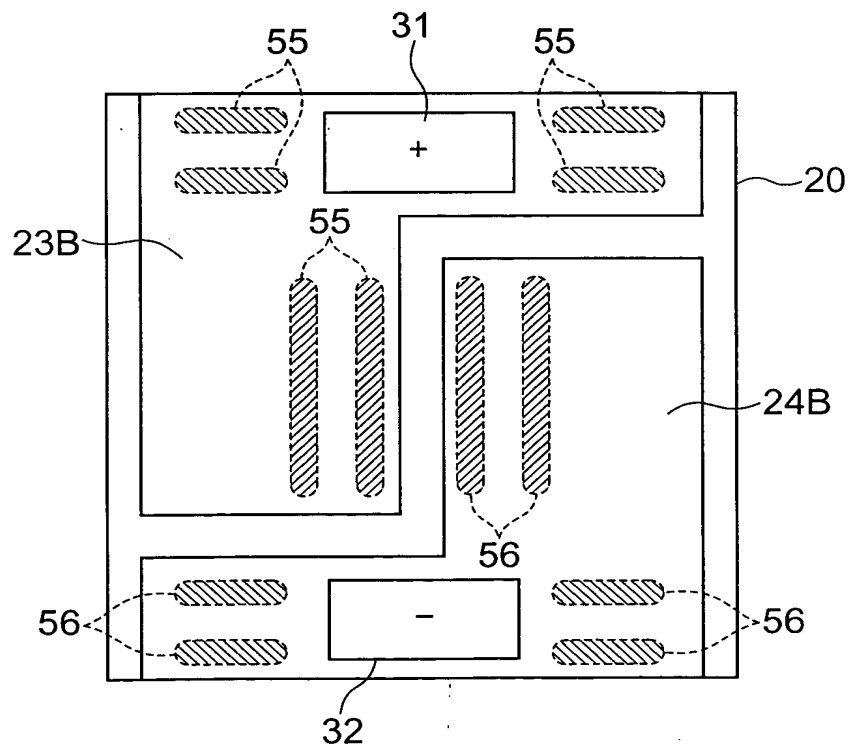


FIG. 15

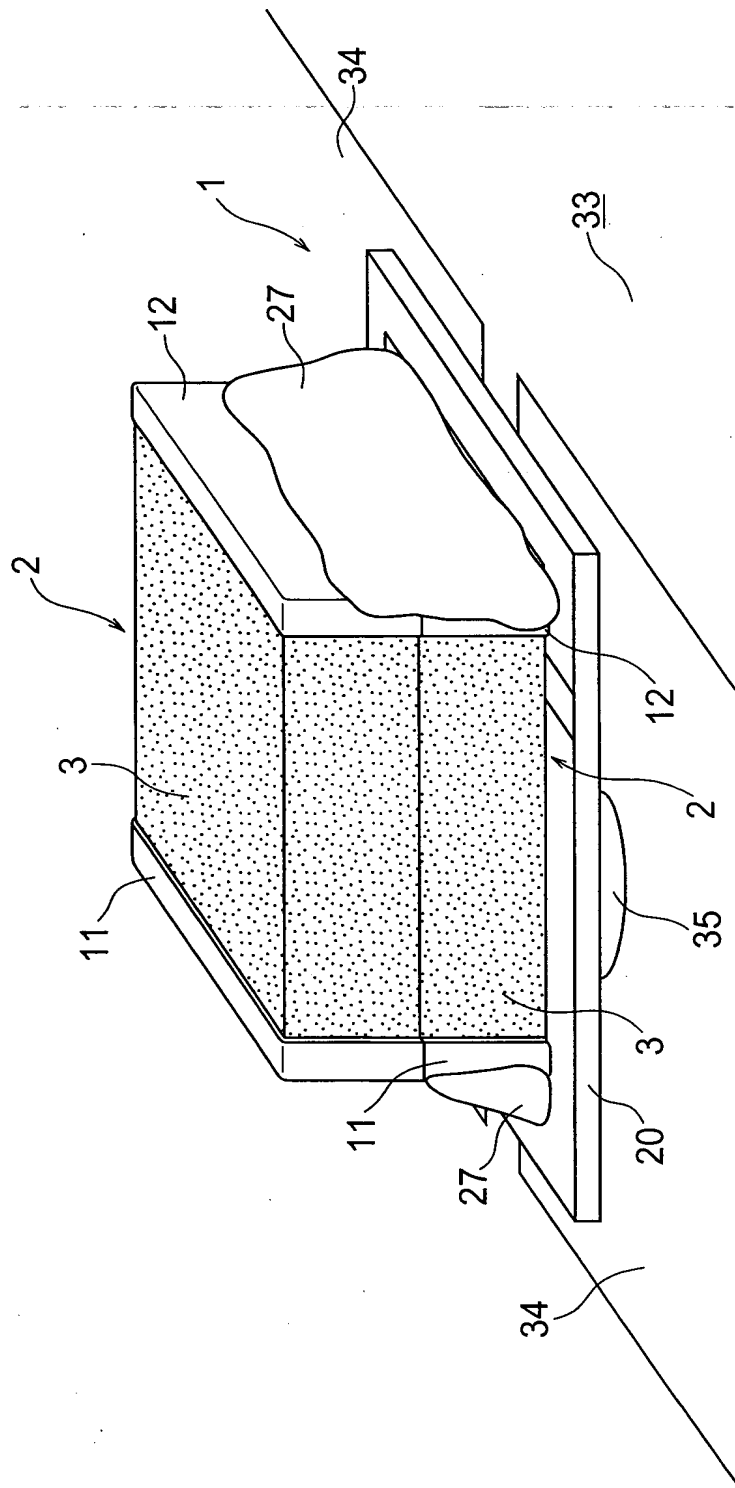


FIG. 16

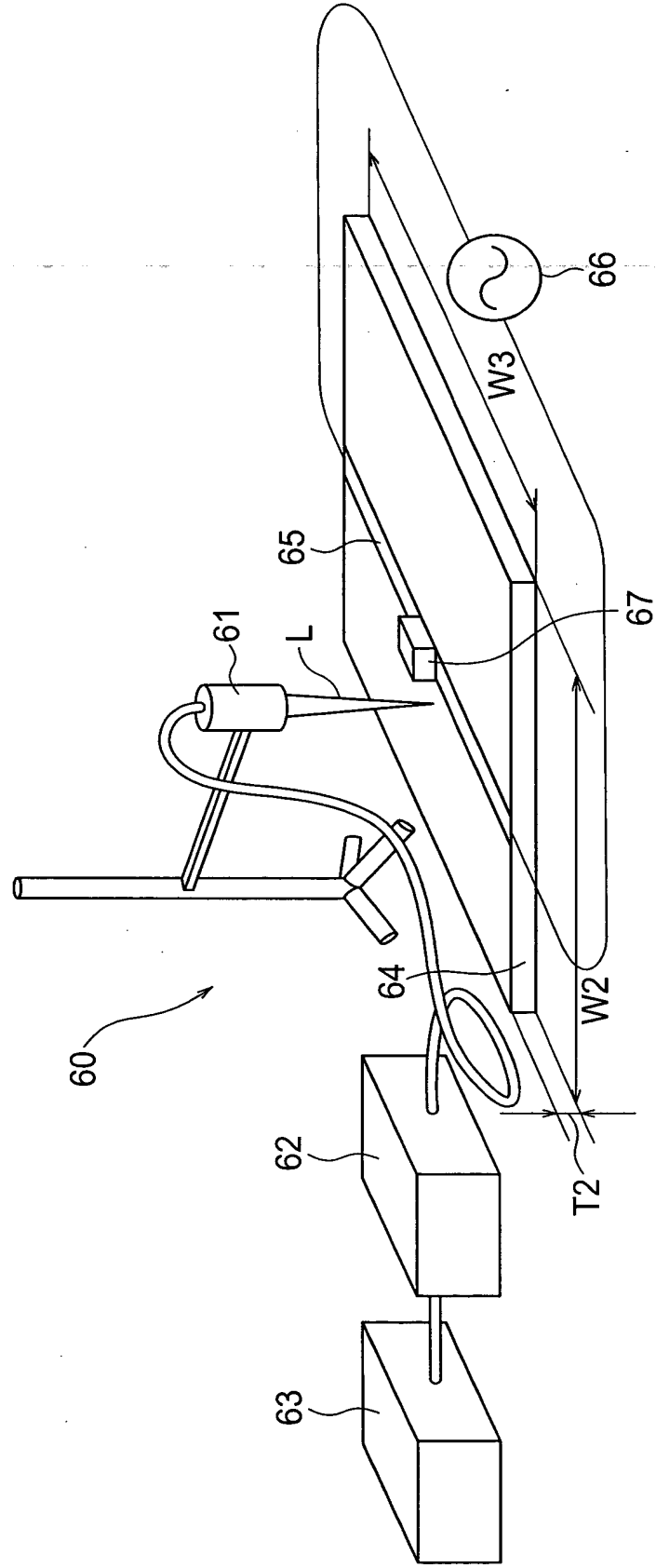


FIG. 17A

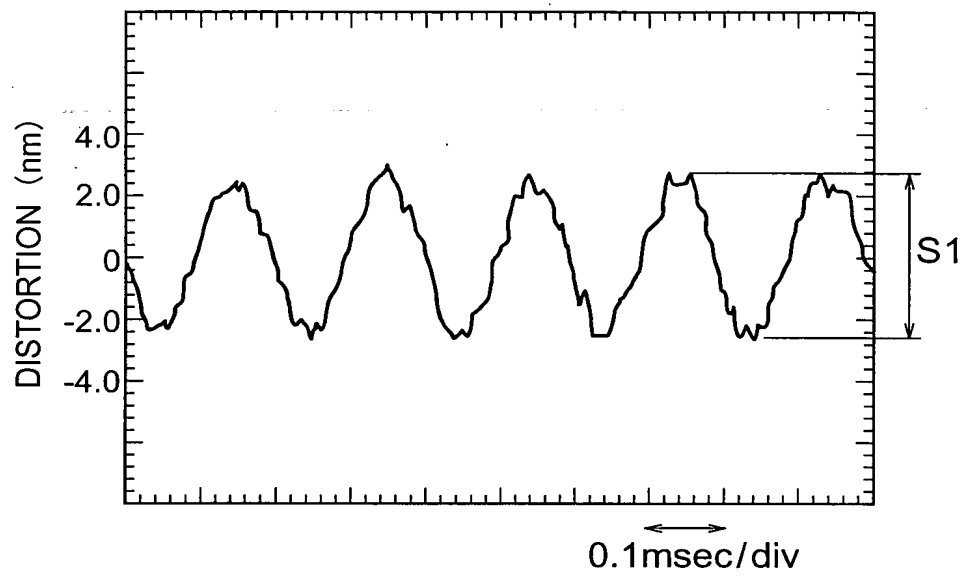


FIG. 17B

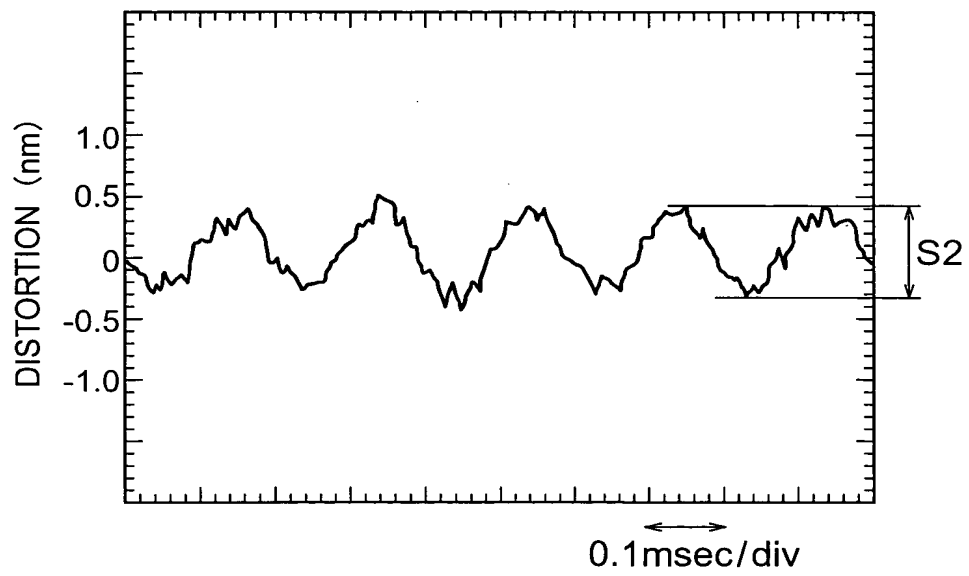


FIG. 18

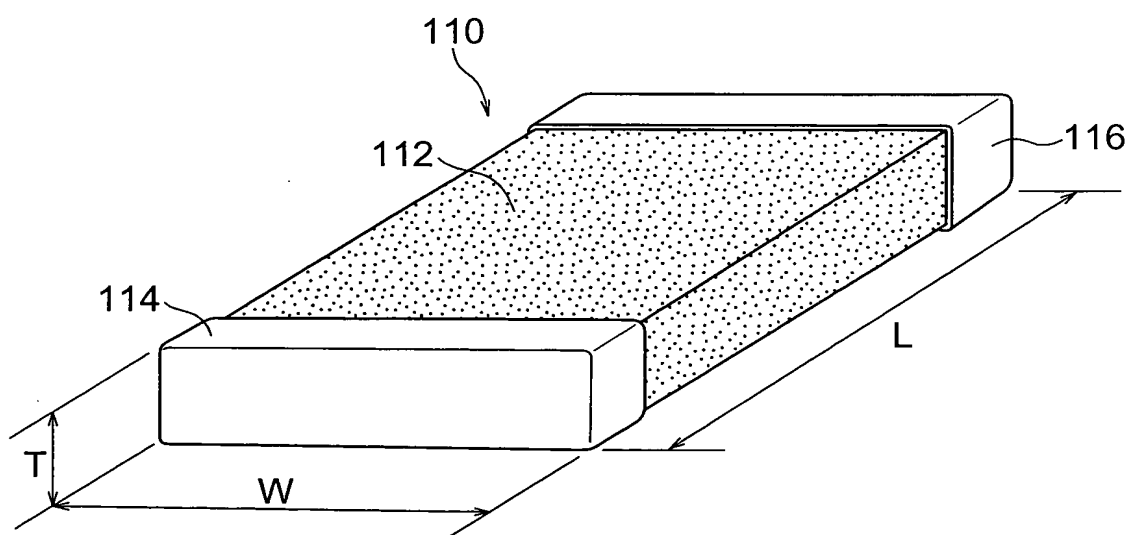


FIG. 19
PRIOR ART

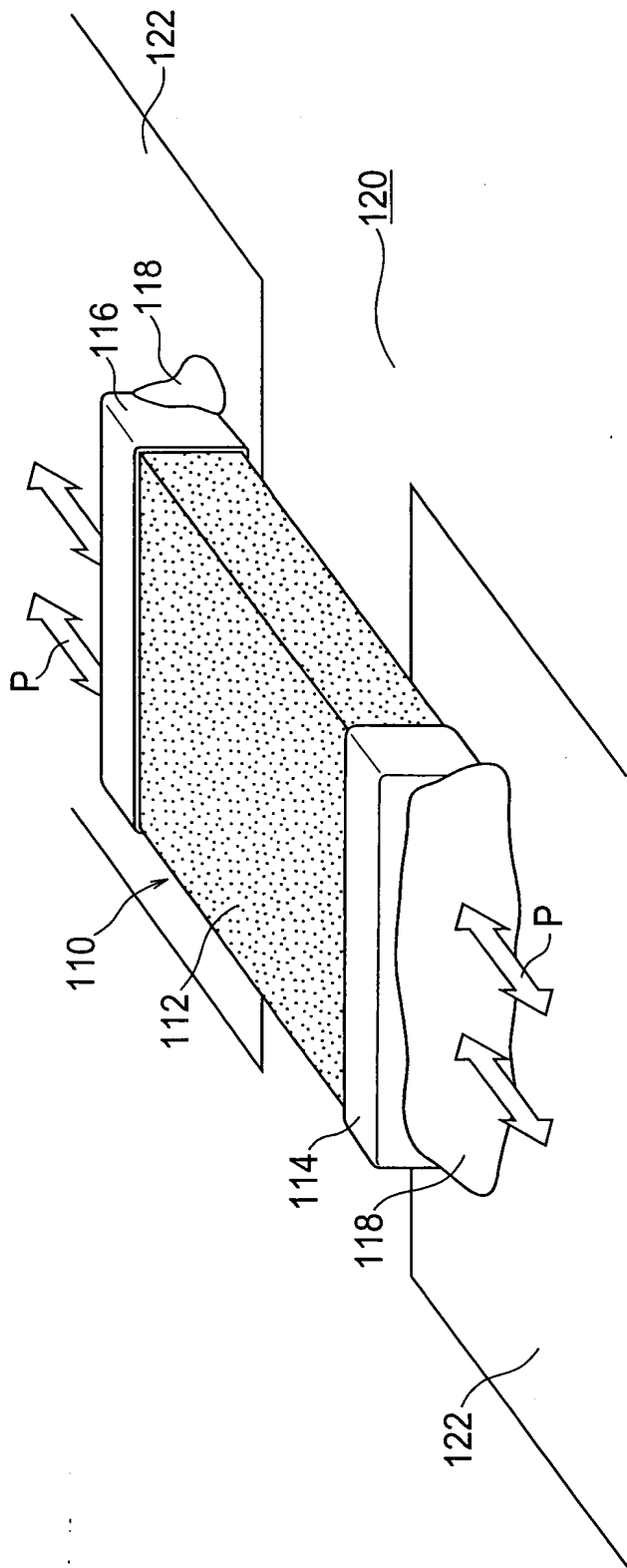


FIG. 20
PRIOR ART

